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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/066,651 | 02/06/2002 | Joo-Seon Kim | Q64314 | 4497 |

7590 12/19/2005

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| TORRES, JOSEPH D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/066,651 | KIM, JOO-SEON | |
| | Examiner | Art Unit | |
| | Joseph D. Torres | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-17,19-22,28-31,33 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17* is/are allowed.

6)☒ Claim(s) *1,4-16,19-22,28-31,33 and 36* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

1. The Applicant contends, "a Supplemental Application Data Sheet supplying the inventor's P.O. address is filed concurrently." The Examiner asserts that no Supplemental Application Data Sheet has been received by the Office to date, hence the Examiner maintains the previous objection.

### *Response to Arguments*

2. Applicant's arguments filed 09/26/2005 have been fully considered but they are not persuasive.

The Examiner summarizes the rejection of claims 1, 10 and 15, below:
Massoudi teaches a storing part (Figure 1A in Massoudi is a storing part); a calculation part for calculating an error location and an error value from 2m-bit data from the storing part wherein m is an integer value (Correction Engine 608 and Correction Circuit 602 in Figure 6 of Massoudi is a calculation part for calculating an error location and an error value from 2m bit data from the storing part; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi; col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error

locations and error values); and a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part to output a decoded signal (Correction Control Circuitry 606 in Figure 6 of Massoudi is a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part, Correction Engine 608 and Correction Circuit 602, to output a decoded signal to Correction Buffer 612; See col. 9, lines 31-67 and col. 10, lines 1-36 in Massoudi);

and the calculation part comprises:

a first RS core for calculating a first error location and a first error value from the data read from the storing part (Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 in Figure 6 of Massoudi comprise a first RS core for calculating a first error location and a first error value from the data read from the storing part; Note: col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error locations and error values; more specifically, col. 8, lines 27-33 in Massoudi teaches that the first RS core comprising Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 is used for calculating a first row error location and a first row error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 in Figure 6 of Massoudi comprise a second RS core

for calculating a second error location and a second error value from the data read from the storing part; more specifically, col. 9, lines 31-42 in Massoudi teaches that the second RS core comprising Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 is used for calculating a second column error location and a second column error value from the data read from the storing part), wherein the control part alternately enables the first RS core and the second RS core to correct the error and update the data (Steps 502-508 in Figure 5 of Massoudi teach that the control part alternately enables the first row RS core and the second column RS core to correct the error and update the data).

The Applicant contends, "Neither Massoudi nor Fujita disclose any RS cores which are ultimately enabled by a control part to correct the error and update the data as claimed". The Examiner disagrees and asserts that steps 502-508 in Figure 5 of Massoudi teach that the control part alternately enables the first row RS core and the second column RS core to correct the error and update the data.

The Applicant contends, "Regarding claims 31, 33 and 36, claims 31, 33 and 36 are allowable over the cited references based on at least their dependencies as well as for their additionally recited features. That is, the cited references do not teach or suggest a number 'sm" which may be appropriately determined according to a data representation method and which represents an amount of data, as recited in claims 31, 33 and 36".

The Examiner disagrees and asserts that Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence m=768 for column data having 2m=1536 data bits. In addition, row data has 172 bytes, i.e., 1376 bits, hence m= 688 for row data having 2m=1376 data bits. The integer m is different for column and row data is selcted according to either a column or a row data representation method.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Massoudi; Firooz (US 6363511 B1).

35 U.S.C. 102(e) rejection of claims 1 and 10.

Massoudi teaches a storing part (Figure 1A in Massoudi is a storing part); a calculation part for calculating an error location and an error value from 2m-bit data from the storing part wherein m is an integer value (Correction Engine 608 and Correction Circuit 602 in Figure 6 of Massoudi is a calculation part for calculating an error location and an error value from 2m bit data from the storing part; Note: Figure 2B in Massoudi teaches that

column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi; col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error locations and error values); and a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part to output a decoded signal (Correction Control Circuitry 606 in Figure 6 of Massoudi is a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part, Correction Engine 608 and Correction Circuit 602, to output a decoded signal to Correction Buffer 612; See col. 9, lines 31-67 and col. 10, lines 1-36 in Massoudi);

and the calculation part comprises:

a first RS core for calculating a first error location and a first error value from the data read from the storing part (Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 in Figure 6 of Massoudi comprise a first RS core for calculating a first error location and a first error value from the data read from the storing part; Note: col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error locations and error values; more specifically, col. 8, lines 27-33 in Massoudi teaches that the first RS core comprising Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 is used for calculating a first row error location and a first row

error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 in Figure 6 of Massoudi comprise a second RS core for calculating a second error location and a second error value from the data read from the storing part; more specifically, col. 9, lines 31-42 in Massoudi teaches that the second RS core comprising Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 is used for calculating a second column error location and a second column error value from the data read from the storing part), wherein the control part alternately enables the first RS core and the second RS core to correct the error and update the data (Steps 502-508 in Figure 5 of Massoudi teach that the control part alternately enables the first row RS core and the second column RS core to correct the error and update the data).

Note: Correction Control Circuit in Figure 6 of Massoudi is a first RS core control part for controlling the first RS core under the control of the main control part and Repeat Correction Manager 812 in Correction Control Circuit in Figures 6 & 8 of Massoudi is second RS core control part for controlling the second RS core under the control of the main control part.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 4-9, 11-16, 19-22, 28-31, 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Massoudi; Firooz (US 6363511 B1) in view of Fujita; Hachiro et al. (US 6131178 A, hereafter referred to as Fujita).

35 U.S.C. 103(a) rejection of claims 4 and 11.

Massoudi substantially teaches the claimed invention described in claims 1, 3 and 10 (as rejected above). In addition, Massoudi teaches a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Row Syndrome Generator Circuitry 604 in Figure 6 of Massoudi is a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part); a first errata location polynomial calculation part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the first errata location

polynomial and the delayed first syndrome polynomial (Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi output the first errata location polynomial and the delayed first syndrome polynomial); and a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial (col. 6, lines 52-54 in Massoudi teach that the Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi generates row erasure pointers, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial; Note: a row erasure pointer is a first error flag).

However Massoudi does not explicitly teach the specific use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial.

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first errata location polynomial from the calculated eraser location

polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Massoudi with the teachings of Fujita by including use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial would have provided the opportunity to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 5.

The syndrome equations in claim 5 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claims 6 and 12.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1, 3 and 4 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 7.

Massoudi teaches a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial (Correction Circuitry 602 in Figure 6 is a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

35 U.S.C. 103(a) rejection of claim 8.

The syndrome equations in claim 8 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 9.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1 and 3-8 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 13.

Massoudi substantially teaches the claimed invention described in claims 1 and 3-12 (as rejected above). In addition, Massoudi teaches a second syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part (Correction Circuitry 602 in Figure 6 of Massoudi is a second errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a first error location and a second error value from the second errata location polynomial and the delayed first syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

However Massoudi does not explicitly teach the specific use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial.

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Massoudi with the teachings of Fujita by including use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome

polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial would have provided the opportunity to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 14.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1 and 3-13 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13. This modification would have been obvious to one of ordinary skill in the art, at the

time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 15.

Massoudi teaches a storing part (Figure 1A in Massoudi is a storing part); a calculation part for calculating an error location and an error value from 2m-bit data from the storing part wherein m is an integer value (Correction Engine 608 and Correction Circuit 602 in Figure 6 of Massoudi is a calculation part for calculating an error location and an error value from 2m bit data from the storing part; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi; col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error locations and error values); and a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part to output a decoded signal (Correction Control Circuitry 606 in Figure 6 of Massoudi is a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part, Correction Engine 608 and Correction Circuit 602, to output a decoded signal to Correction Buffer 612; See col. 9, lines 31-67 and col. 10, lines 1-36 in Massoudi);

and the calculation part comprises:

a first RS core for calculating a first error location and a first error value from the data read from the storing part (Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 in Figure 6 of Massoudi comprise a first RS core for calculating a first error location and a first error value from the data read from the storing part; Note: col. 7, lines 34-36 in Massoudi teach the use of Reed-Solomon Codes, one of ordinary skill in the art at the time the invention was made would have known that Reed-Solomon codes are error corrected by finding error locations and error values; more specifically, col. 8, lines 27-33 in Massoudi teaches that the first RS core comprising Row Syndrome Generator Circuitry 604, Correction Engine 608 and On-The Fly Row Correction 410 is used for calculating a first row error location and a first row error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 in Figure 6 of Massoudi comprise a second RS core for calculating a second error location and a second error value from the data read from the storing part; more specifically, col. 9, lines 31-42 in Massoudi teaches that the second RS core comprising Column and EDC Syndrome Generator Circuitry 412, Correction Engine 608 and Correction Circuitry 602 is used for calculating a second column error location and a second column error value from the data read from the storing part), wherein the control part alternately enables the first RS core and the second RS core to correct the error and update the data (Steps 502-508 in Figure 5 of

Massoudi teach that the control part alternately enables the first row RS core and the second column RS core to correct the error and update the data).

Note: Correction Control Circuit in Figure 6 of Massoudi is a first RS core control part for controlling the first RS core under the control of the main control part and Repeat Correction Manager 812 in Correction Control Circuit in Figures 6 & 8 of Massoudi is second RS core control part for controlling the second RS core under the control of the main control part.

However Massoudi does not explicitly teach the specific use of reading data to be decoded and an eraser flag (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part).

Fujita, in an analogous art, teaches use of reading data to be decoded and an eraser flag.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Massoudi with the teachings of Fujita by including use of reading data to be decoded and an eraser flag. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of reading data to be decoded and an eraser flag would have provided increased error correction capabilities (Note: one of ordinary skill in the art at the time the invention was made would have recognized that a Reed-Solomon code is capable of correcting twice as many erasures as errors).

35 U.S.C. 103(a) rejection of claim 16.

Figure 6 in Massoudi is a Reed-Solomon decoder; see col. 7, lines 35-40 in Massoudi; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi.

35 U.S.C. 103(a) rejection of claim 19.

Massoudi teaches a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Row Syndrome Generator Circuitry 604 in Figure 6 of Massoudi is a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part); a first errata location polynomial calculation part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the first errata location polynomial and the delayed first syndrome polynomial (Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi output the first errata location polynomial and the delayed first syndrome polynomial); and a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial (col. 6, lines 52-54 in Massoudi teach that the Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi

generates row erasure pointers, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial; Note: a row erasure pointer is a first error flag).

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 20.

The syndrome equations in claim 20 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 21.

Massoudi teaches a second syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part (Correction Circuitry 602 in Figure 6 of Massoudi is a second errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a first error location and a second error value from the second errata location polynomial and the delayed first syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24

in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 22.

The syndrome equations in claim 22 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claims 28 and 29.

The syndrome equations in claims 28 and 29 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 30.

Massoudi teaches a first RS core for calculating a first error location and a first error value from the data read from the storing part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first RS core for calculating a first error location and a first error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Correction Circuitry 602 in Figure 6 of Massoudi is a second RS core for calculating a second error location and a second error value from the data read from the storing part).

35 U.S.C. 103(a) rejection of claims 31, 33 and 36.

Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence m=768 for column data having 2m=1536 data bits. In addition, row data has 172 bytes, i.e., 1376 bits, hence m= 688 for row data having 2m=1376 data bits. The integer m is different for column and row data is selcted according to either a column or a row data representation method.

***Allowable Subject Matter***

5. Claim 17 is allowed.

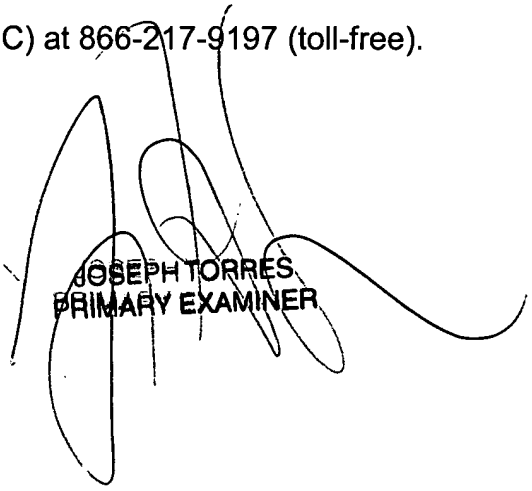
Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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